AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 5, as follows:

The present invention relates to a buffer circuit. ~~More specifically~~ Specifically, the invention relates to a buffer circuit ~~suitably applied to~~ suitable for a buffer for driving a clock signal and a semiconductor integrated circuit.

Please amend the paragraph beginning at page 1, line 10, as follows:

Recently, in [[a]] semiconductor integrated circuits such as high-speed CMOS circuits, [[an]] the operating frequency of the circuits has become higher and hence the length of one clock cycle ~~is~~ has been reduced. Further, as integration density and function level of a semiconductor integrated circuit become higher, [[a]] clock interconnections become[[s]] longer. In a semiconductor integrated circuit ~~provided~~ with clock synchronous circuits, such as latches or registers, which also perform sampling of data in response to a clock transition, a clock tree system is employed. This [[as a]] technique allows for matching delays from a clock source, such as a clock input pin or an internal clock generation circuit, to the respective clock synchronous circuits, and thereby performing clock distribution. In the clock tree system, as shown in Fig. 12, clock buffer circuits (also referred to as "CTS (Clock Tree Synthesis) buffer circuits) INV101 to INV117 are disposed along clock propagation paths. A conventional clock buffer circuit is comprised of a PMOS transistor and an NMOS transistor. In case wherein the clock buffer circuit is composed of a CMOS inverter, an input signal is supplied to commonly coupled gates of a PMOS transistor and an NMOS transistor connected in series between a high-potential power supply and a low-potential power supply, and an output signal of the

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clock buffer circuit is outputted from a connection point between a drain of the PMOS transistor and the drain of the NMOS transistor. For speeding up a high-level output driven by the PMOS transistor which is turned on, a size of the PMOS transistor is made large, while the size of the NMOS transistor is made small and hence a $\beta p/\beta n$ ratio is made large, thereby achieving speeding up the high-level output, where the $\beta p/\beta n$ ratio is a ratio of gain coefficients between the PMOS transistor and the NMOS transistor that constitute the CMOS inverter. The β is given by $(\mu\varepsilon/t_{ox})(W/L)$, where μ represents a carrier mobility, ε represents a dielectric constant of a gate dielectric film, t_{ox} represents a thickness of the gate dielectric film, W represents a channel width, and L represents a channel length. However, when achieving the speeding up by increasing the $\beta p/\beta n$ ratio, the size of the NMOS transistor must be made especially smaller because of a cell size constraint or the like, so that a fall time of an output waveform to a low level becomes slow. Further, if the $\beta p/\beta n$ ratio is increased by reducing the size of the NMOS transistor, sensitivity to manufacturing variations is increased, as a result of which, an operation margin will be also extremely deteriorated.

Please amend the paragraph beginning at page 3, line 25, as follows:

If a propagation delay time of each buffer circuit, inserted in a clock path for delay adjustment, is long and a plurality of buffer circuits are inserted from a clock source to a clock destination, the delays caused by the buffer circuits greatly affect [[an]] the operation timing of a clock synchronous circuit, such as a latch or register, which is [[a]] the destination of clock ~~destination~~ signal. In a CMOS circuit driven with an operating frequency exceeding 100 MHz, for example, one clock cycle (tCK) is less than 10 nanoseconds. As shown in Fig. 12, four buffers for delay adjustment are inserted [[in]] into each clock tree. If the propagation delay

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time per buffer is assumed to be roughly 600 ps (pico-seconds), 2.4 ns (nano-seconds) of time is spent [[for]] by the buffers [[for]] in delay adjustment and hence a sufficient timing margin in a latch, register or the like, which is the destination of the clock ~~destination~~ signal, may not be left.

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